

BIAX Corporation v. Intel
Civil Action No. 2:05-cv-184-TJW

EXHIBIT 5
(PART 1)
FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

US005765037A

United States Patent [19][11] **Patent Number:** **5,765,037****Morrison et al.**[45] **Date of Patent:** **Jun. 9, 1998****[54] SYSTEM FOR EXECUTING INSTRUCTIONS WITH DELAYED FIRING TIMES**

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 Boulder, all of Colo.

[73] Assignee: **Biax Corporation**, Palm Beach
 Gardens, Fla.

[21] Appl. No.: **480,841**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 254,687, Jun. 6, 1994, Pat. No. 5,517, 628, which is a division of Ser. No. 93,794, Jul. 19, 1993, abandoned, which is a continuation of Ser. No. 913,736, Jul. 14, 1992, abandoned, which is a continuation of Ser. No. 560,093, Jul. 30, 1990, abandoned, which is a division of Ser. No. 372,247, Jun. 26, 1989, Pat. No. 5,021,945, which is a division of Ser. No. 794,221, Oct. 31, 1985, Pat. No. 4,847,755.

[51] Int. Cl.⁶ **G06F 9/40**

[52] U.S. Cl. **395/557; 395/391; 395/559;**
395/800.21; 395/580

[58] Field of Search **395/375, 550,**
395/391, 595, 557, 559, 800.21, 580

[56] References Cited**U.S. PATENT DOCUMENTS**

4,200,912	4/1980	Harrington et al.	395/742
4,229,790	10/1980	Gilliland et al.	395/671
4,247,894	1/1981	Beismann et al.	395/737
4,250,546	2/1981	Boney et al.	395/735
4,342,078	7/1982	Tredennick et al.	395/387
4,430,707	2/1984	Kim	395/670
4,466,061	8/1984	DeSantis	395/676
4,532,589	7/1985	Shintani et al.	395/393
4,598,400	7/1986	Hillis	370/400
4,833,599	5/1989	Colwell et al.	395/583

OTHER PUBLICATIONS

Chang et al., "801 Storage: Architecture and Programming," IBM T.J. Watson Research Center, 1988, 0734-2071/88/0200-0028, pp. 29-50.

Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler." Second International Conference on ASPLOS-II, Oct. 5-8, 1987, pp. 1-23.

Davis, "Tomorrow's Computers—The Challenges," IEEE Spectrum, Nov. 1981?, pp. 94-99.

Ellis, "Bulldog: A Compiler for VLIW Architectures," MIT, 1986.

Gross et al., "Optimizing Delayed Branches," IEEE, 15th Annual Workshop on Microprogramming, 1982, 0194-1895/82/0000/0014, pp. 114-120.

Hagiwara et al., "A Dynamically Microprogrammable Computer with Low-Level Parallelism," IEEE, Jul. 1980, 0018-9340/80/0700-0577, vol. C-29, No. 7, pp. 577-594.

Hennessy et al., "The MIPS Machine," IEEE, 1982, CH1739-2/82/0000-0002, vol. C-24, pp. 2-7.

Hennessy et al., "Postpass Code Optimization of Pipeline Constraints," ACM Transactions on Programming Languages and Systems, Jul. 1983, ACM 0164-0925/83/0700-0422, vol. 5, No. 3, pp. 442-448.

(List continued on next page.)

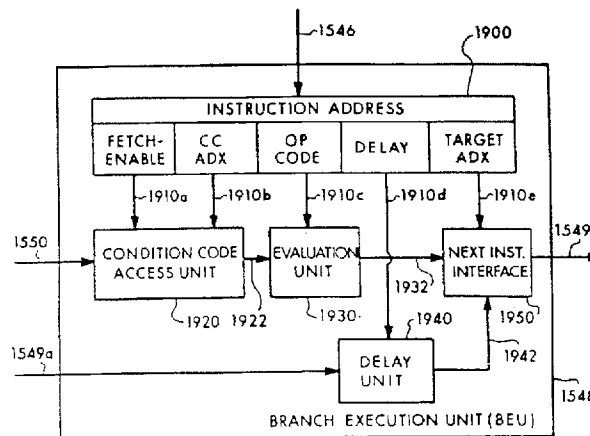
Primary Examiner—Kenneth S. Kim

Attorney, Agent, or Firm—Fish & Richardson P.C.

[57] ABSTRACT

A system and method reorder instructions for effecting faster branch execution. A processor element is coupled to receive stored instructions in a first order, and to process the received instructions in a different order, the processing occurring after each stored instruction of a first type is issued, and after a delay time, after each stored instruction of a second type is issued. The delay time is based on a delay value associated with the second type of instructions. In particular, the instructions include branch and non-branch instructions wherein firing time information identifies a time of execution of the branch instruction which is a variable number of instructions cycles prior to a time of execution of a last to be executed instruction in a basic block. Accordingly, branch instructions can be completely executed no later than during the processing of the last to be executed non-branch instruction in the basic block thereby speeding up overall processing of the software program by the system.

29 Claims, 17 Drawing Sheets



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OTHER PUBLICATIONS

Hennessy, "VLSI Processor Architecture," *IEEE Transactions on Computers*, 0018-9340/84/1200-1221, vol. C-33, No. 12, pp. 1221-1246, 1984.

Hennessy, "VLSI RISC Processors," *VLSI Systems Design*, Oct. 1985, pp. 22-24, 28, 32.

McDowell et al., "Processor Scheduling for Linearly Connected Parallel Processors," *IEEE Transactions on Computers*, 1986, 0018-9340/86/0700-0632, vol. C-35, No. 7, pp. 633-638.

McDowell, "A Simple Architecture for Low Level Parallelism," *IEEE*, 1983, 0190-3918/83/0000/0472, pp. 472-477.

McDowell, "SIMAC: A Simple Multiple ALU Computer," University of California, San Diego, 1983.

Patterson et al., "The Case for the Reduced Instruction Set Computer," University of California, Berkeley, pp. 25-32.

Patterson, "Reduced Instruction Set Computers," *Communications of the ACM*, Jan. 1985, vol. 28, No. 1, pp. 8-21.

Patterson, "Microprogramming," pp. 50-57.

Radin, "The 801 Minicomputer," *Computer Architecture News*, Apr. 1982, ACM 0-89791-066-4 82/03/0039, vol. 10, No. 2, 39-47.

Tomita et al., "A User-Microprogrammable, Local Host Computer with Low-Level Parallelism," *Communications of the ACM*, 0149-7111/83/0600/0151, pp. 151-157, 1983.

Alpha Architecture Reference Manual, Digital, 1992.

PowerPC 601 RISC Microprocessor User's Manual, IBM, 1993.

Intel MCS-80 User's Manual, Intel, Oct. 1977.

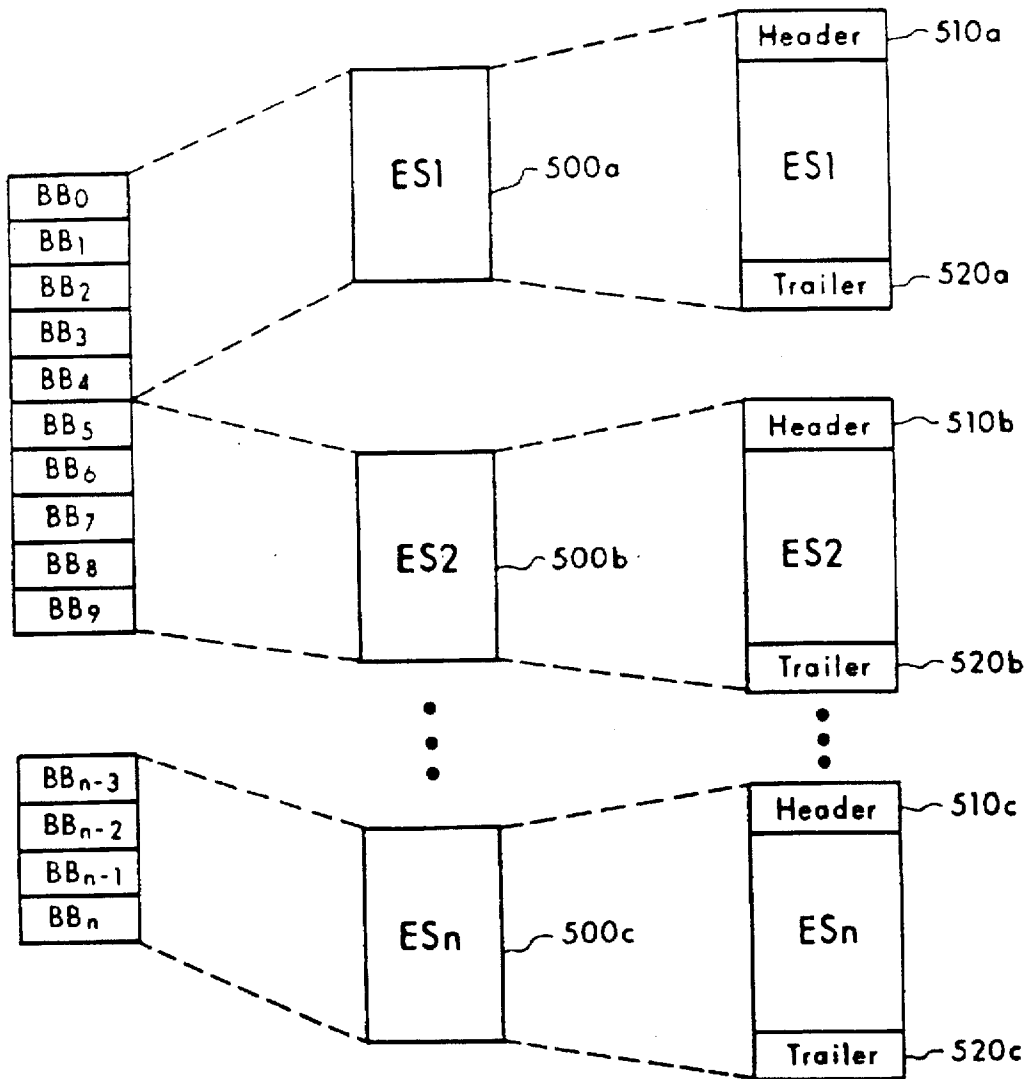
Heinrich, *MIPS Microprocessor R4000 User's Manual*, MIPS Technologies, Inc., 1993.

MC68030 Enhanced 32-Bit Microprocessor User's Manual, Second Edition, Motorola, Inc., 1989.

FIG. 4

IO	LPN ₀	IFT ₀	SCSM ₀
I ₁	LPN ₁	IFT ₁	SCSM ₁
⋮			
I _n	LPN _n	IFT _n	SCSM _n

FIG. 5



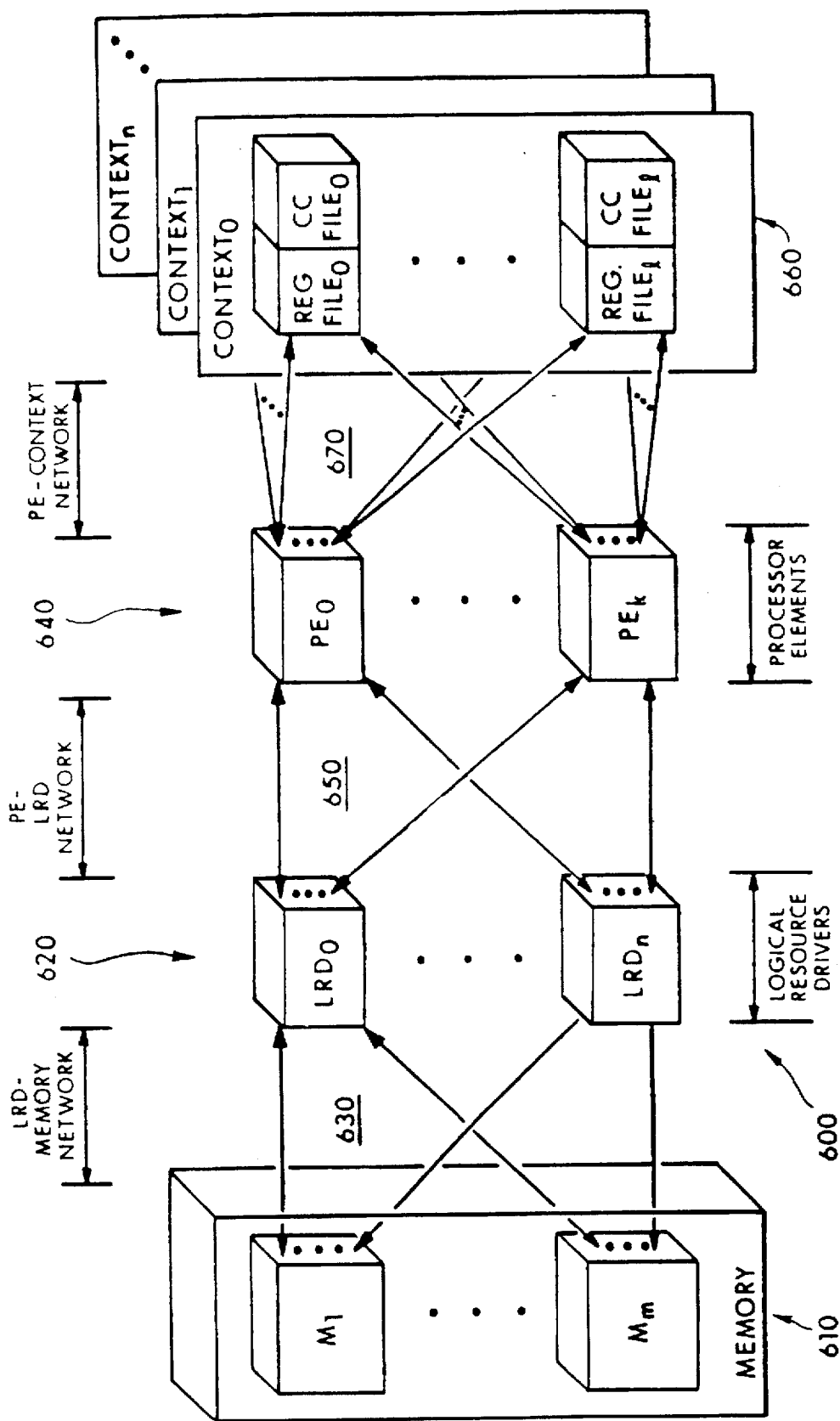


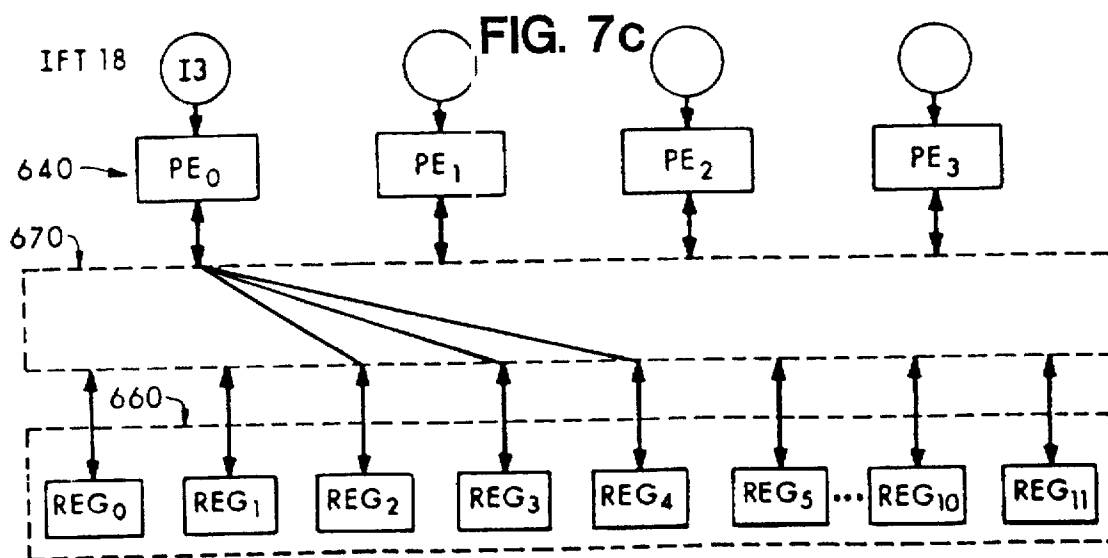
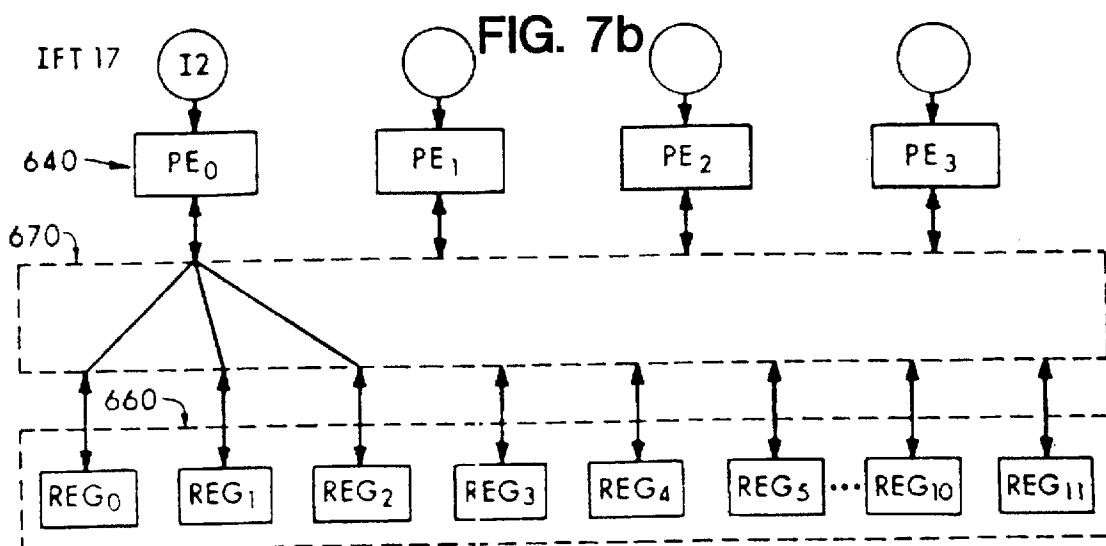
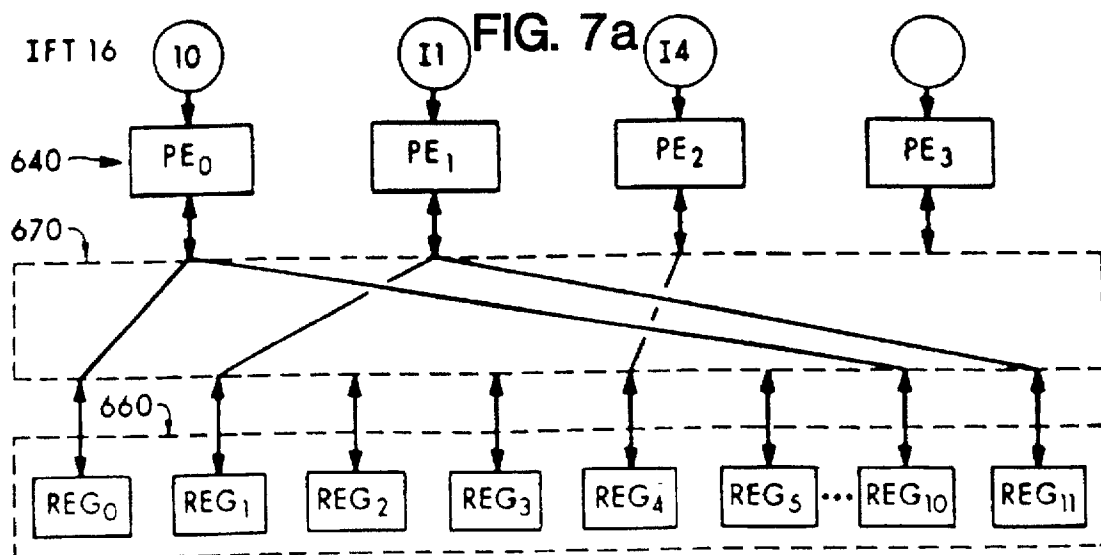
FIG. 6

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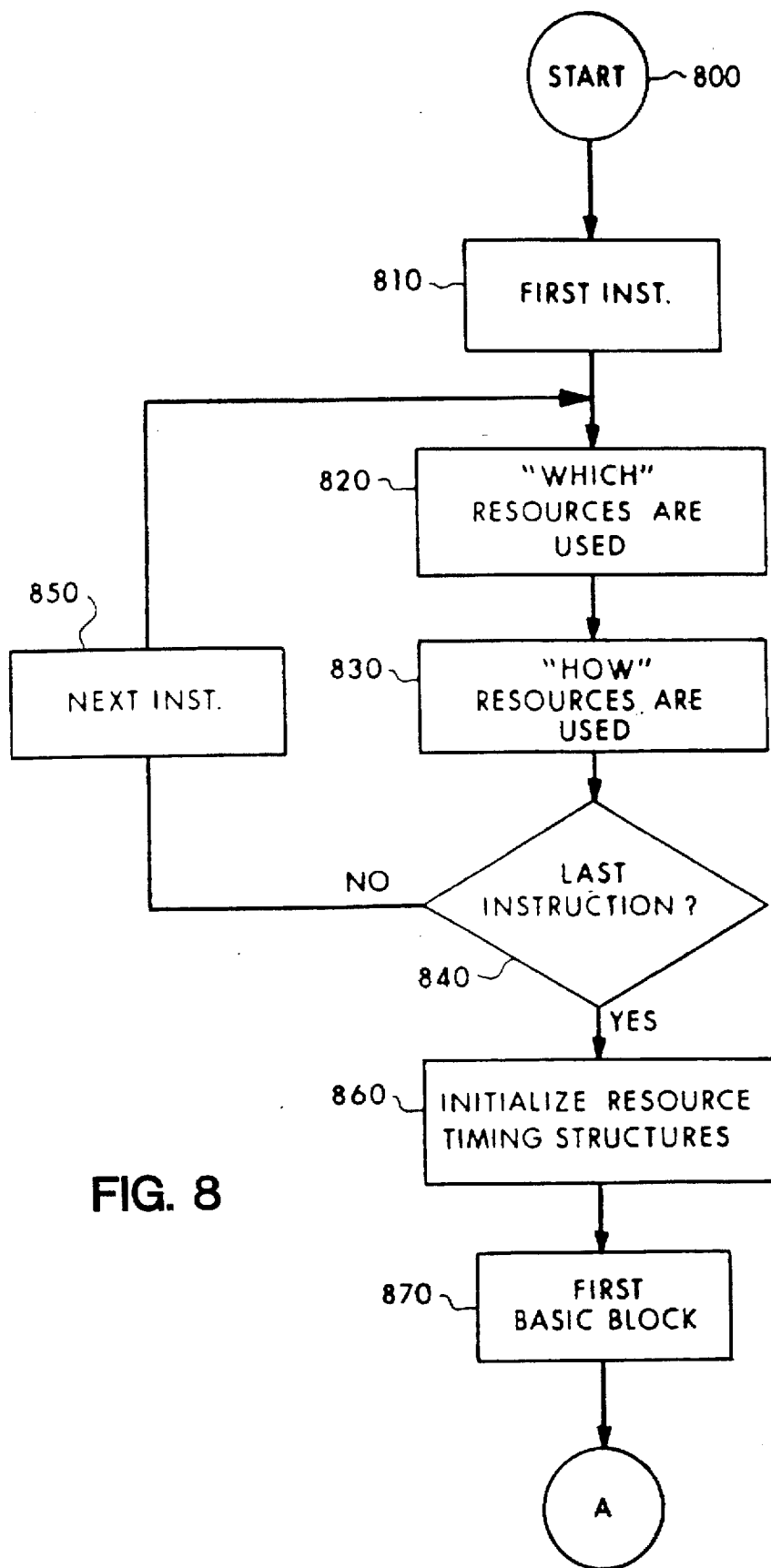


FIG. 8

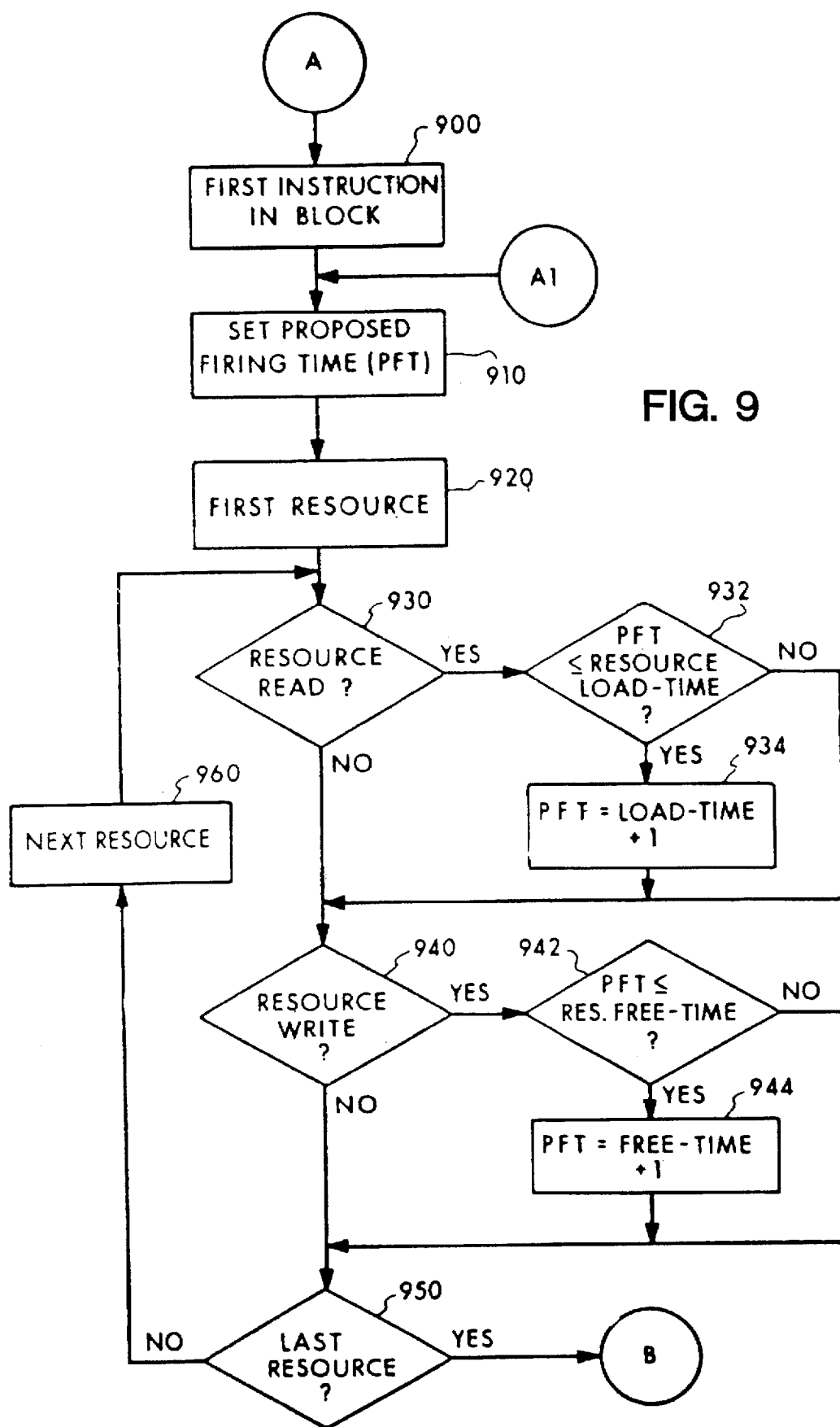
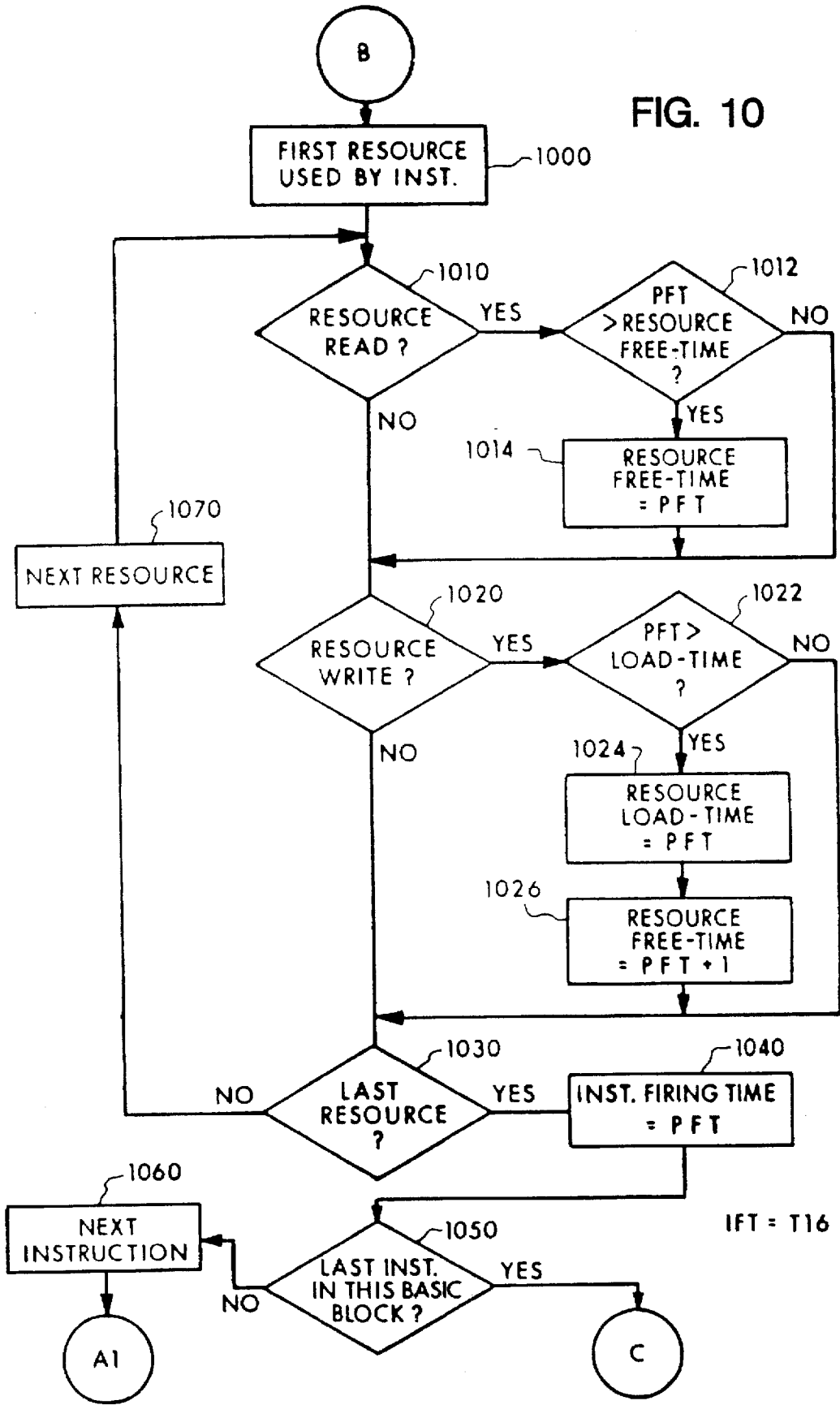
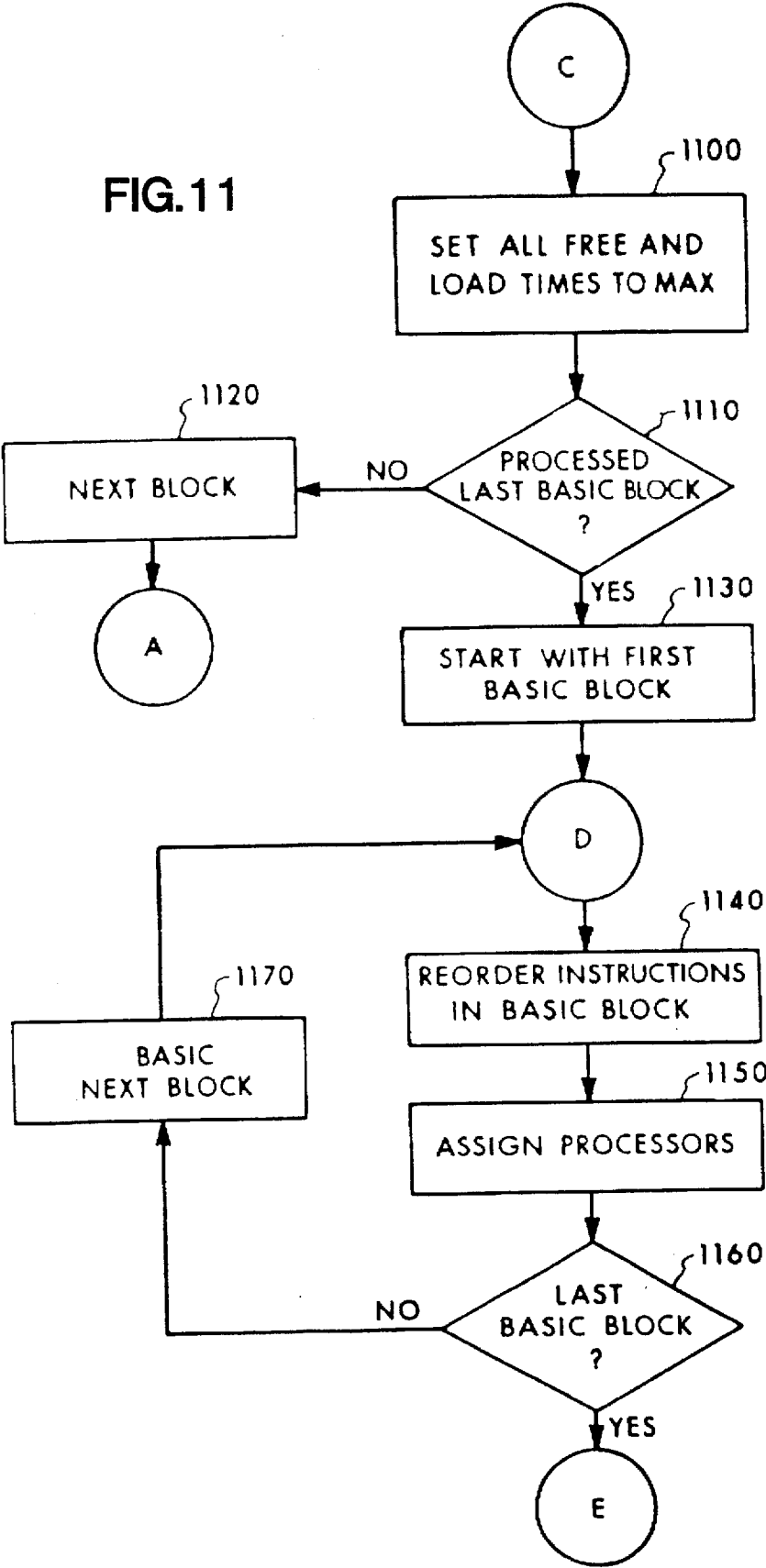


FIG. 10





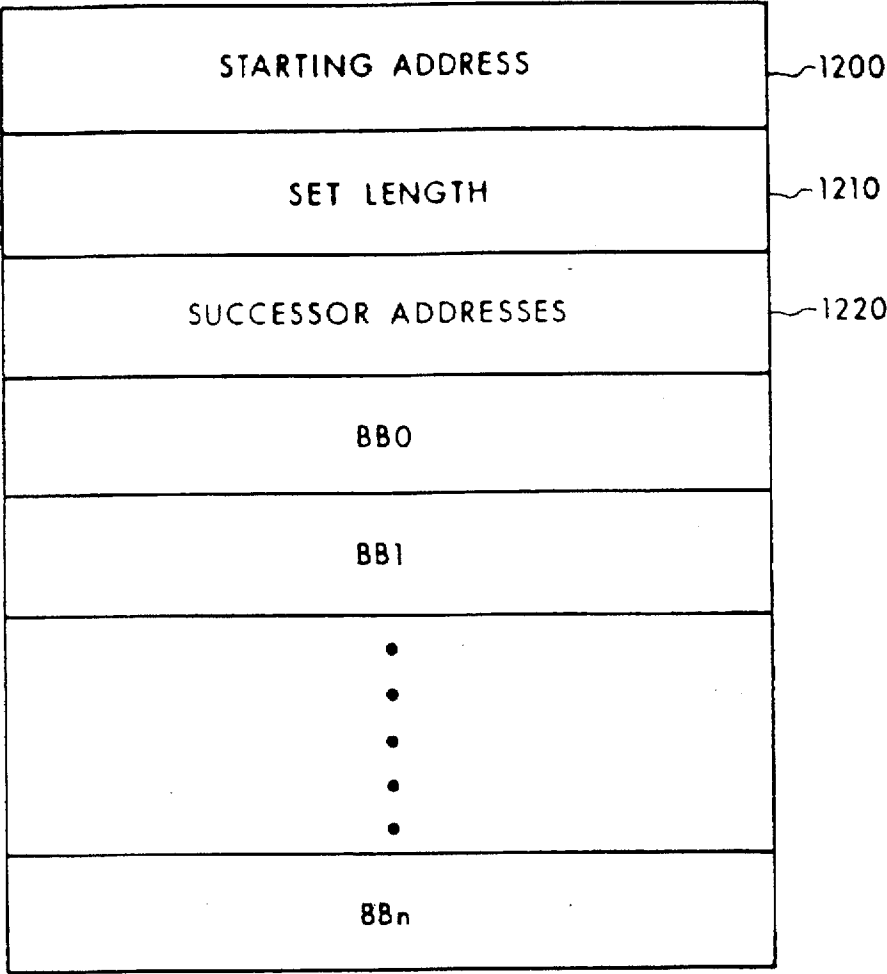


FIG. 12

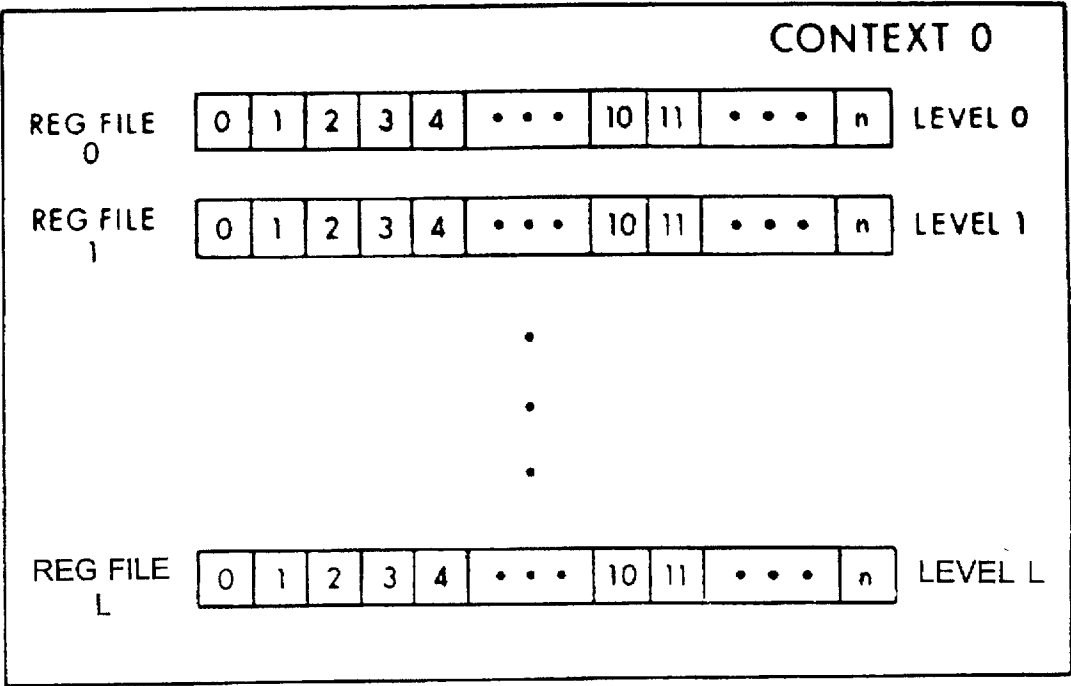


FIG. 13

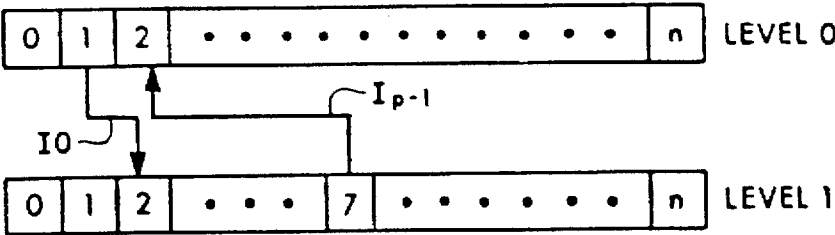


FIG. 14

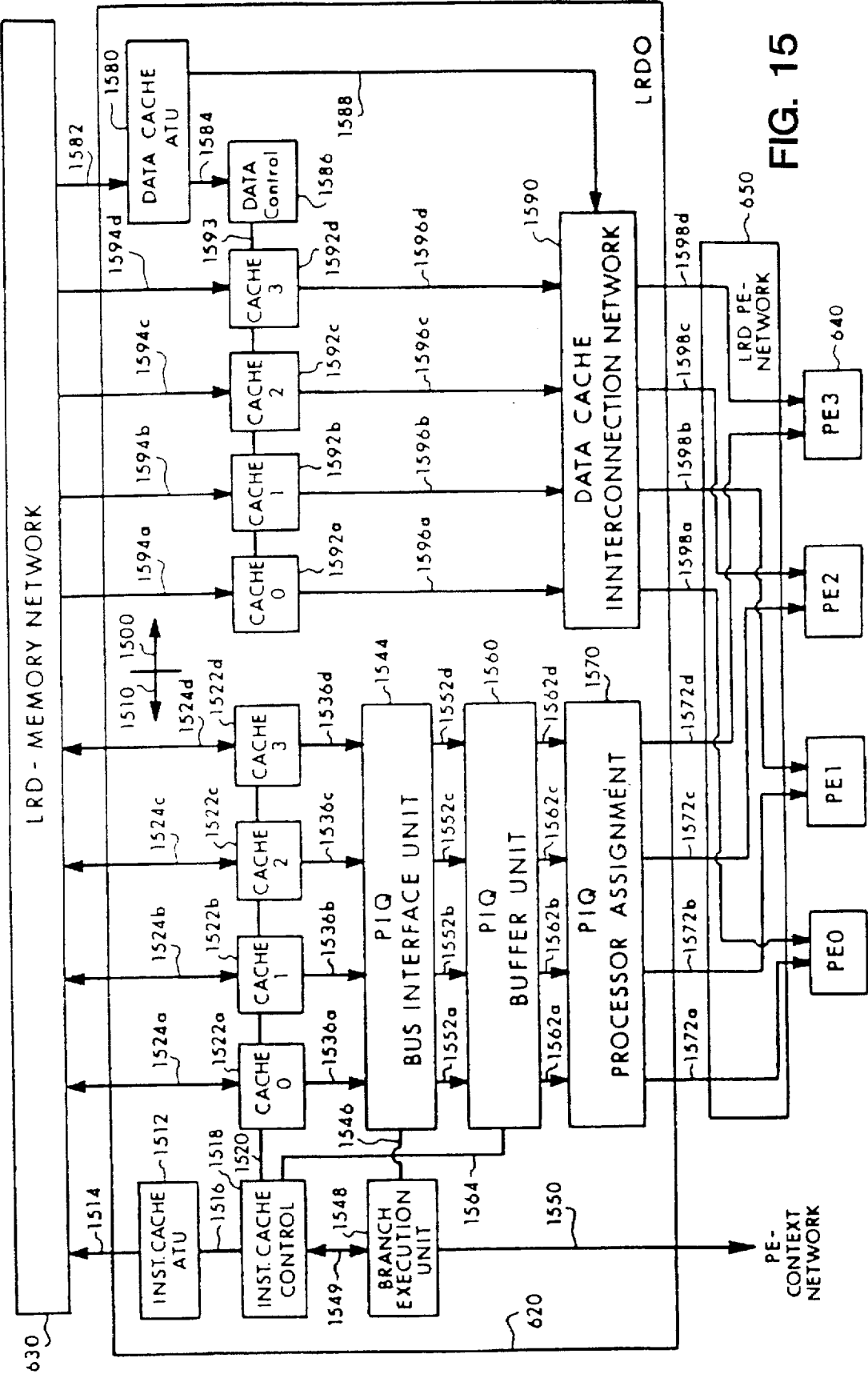


FIG. 15

